Subt A6

What is claimed is:

1. A semiconductor device which comprises;

a substrate, on a main surface of which, interconnect layers made at least of copper are formed along with a predetermined pattern in buried condition;

an etching-stop layer formed on said main surface of said substrate; and

an insulation layer formed on said etching-stop layer,

said semiconductor device further comprises a via-hole provided on a main surfacer of said insulation layer and penetrating through said insulation layer and said etching-stop layer so that a bottom of said via-hole reaches at a surface of said interconnect layer, and wherein a barrier layer continuously covering said main surface of said insulation layer, inside wall surface of said via-hole and surface of said interconnect layer integratedly.

2. A method for forming a via hole of a semiconductor device comprising:

Sub C2

a step of forming a first step via hole in a laminated structure formed by a copper layer, an etching-stop layer formed on a surface of said copper layer, and an insulation layer formed on a surface of said etching-stop layer, thereby a bottom of said first step via hole is stopped at said etching-stop layer;

a step of forming a second step via hole continuous with said first step via hole in said etching-stop layer, thereby a bottom of said second step via hole reaching at a surface of said interconnect layer;

a step of cleaning said second step via hole; and

a step, after said cleaning, of forming a barrier film on said first and second step via holes, by sputtering.

3. A method for forming a via hole of a semiconductor device according to claim2, wherein said step of cleaning said via hole comprises a step for annealing said via hole at a low oxygen partial pressure.

4. A method for forming a via hole of a semiconductor device according to claim 3, wherein said step of cleaning said via hole further comprises a step for treating said via hole with an oxygen plasma, before said step of annealing said via hole at a low oxygen partial pressure.

5. A method for forming a via hole of a semiconductor device according to claim 4, wherein said step of cleaning said via hole further comprises a step for performing wet processing of the via hole after treating said via hole with an oxygen plasma.

6. A method for forming a via hole of a semiconductor device according to claim 3, wherein said step of annealing said via hole at a low oxygen partial pressure is further performed in a sputtering chamber for said sputtering.

7. A method for forming a via hole of a semiconductor device according to claim 6, wherein said step for annealing said via hole at a low oxygen partial pressure is further performed immediately before said sputtering.

8. A method for forming a via hole of a semiconductor device according to claim 7, wherein said semiconductor substrate in the step for annealing said via hole at a low oxygen partial pressure is held in said sputtering chamber at a temperature of 250 ℃ or greater for at least three minutes before said step of forming a barrier film.

9. A method for forming a via hole of a semiconductor device according to claim 8, wherein the oxygen partial pressure when said sputtering is performed is 1 Torr or lower.

10. A method for forming a via hole of a semiconductor device according to claim 8, wherein said step of annealing said via hole at a low oxygen partial pressure is performed in a hydrogen atmosphere.

11. A method for forming a via hole of a semiconductor device according to claim 10, wherein said step of annealing said via hole at a low oxygen partial pressure is performed in an atmosphere in which hydrogen radicals are supplied.